Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-19. (Canceled)

20. (Previously Presented) A semiconductor device having a thin film transistor, the thin film transistor comprising:

a semiconductor layer on an insulating surface, wherein the semiconductor layer has a side recess;

a gate electrode adjacent to the semiconductor layer with a gate insulating film interposed therebetween; and

a source electrode in contact with the semiconductor layer, wherein the source electrode contains a first layer and a second layer, and

wherein the side recess is filled with the first layer, and

wherein the first layer is in contact with the gate insulating layer.

21-27.(Canceled)

28. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the semiconductor layer contains crystalline silicon.

29. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the first layer contains at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony.

30. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the first layer is an alloy of aluminum and germanium.

31. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the second layer contains aluminum.

32. (Canceled)

33. (Previously Presented) The semiconductor device having a thin film transistor according to claim 20, wherein the semiconductor device is an active matrix type EL display device.

34. (Previously Presented) A semiconductor device having a thin film transistor, the thin film transistor comprising:

a semiconductor layer on an insulating surface, wherein the semiconductor layer has a first side recess;

a gate electrode adjacent to the semiconductor layer with a gate insulating film interposed therebetween, wherein the gate electrode has a second side recess; and

a source electrode in contact with the semiconductor layer and a wiring in contact with the gate electrode,

wherein the source electrode contains a first layer and a second layer,

wherein the wiring contains a third layer and a fourth layer,

wherein the first side recess is filled with the first layer,

wherein the second side recess is filled with the third layer, and

wherein the first layer is in contact with the gate insulating layer.

35. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the semiconductor layer contains crystalline silicon.

36. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the first layer contains at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony.

37. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the first layer is an alloy of aluminum and germanium.

38. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the second layer contains aluminum.

39. (Canceled)

40. (Previously Presented) The semiconductor device having a thin film transistor according to claim 34, wherein the semiconductor device is an active matrix type EL display device.

41. (Currently Amended) A semiconductor device having a thin film transistor, the thin film transistor comprising:

a semiconductor layer on an insulating surface, wherein the semiconductor layer has a side recess;

a gate insulating film on the semiconductor layer;

a gate electrode on the gate insulating film;

an interlayer insulating film over at least the gate electrode; and

a source electrode over the interlayer insulating film,

wherein the source electrode is in contact with the semiconductor layer through a contact hole opened in the interlayer insulating film,

wherein the source electrode contains a first layer and a second layer, [[and]]

wherein a part of the first layer and a part of the second layer are located over the interlayer insulating film,

wherein the side recess is filled with the first layer, and

wherein the first layer is in contact with the gate insulating layer.

42. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the semiconductor layer contains crystalline silicon.

43. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the first layer contains at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony.

44. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the first layer is an alloy of aluminum and germanium.

45. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the second layer contains aluminum.

46. (Canceled)

47. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the interlayer insulating film contains at least one selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

48. (Previously Presented) The semiconductor device having a thin film transistor according to claim 41, wherein the semiconductor device is an active matrix type EL display device.

49. (Currently Amended) A semiconductor device having a thin film transistor, the thin film transistor comprising:

a semiconductor layer on an insulating surface, wherein the semiconductor layer has a first side recess;

a gate insulating film on the semiconductor layer;

a gate electrode on the gate insulating film, wherein the gate electrode has a second side recess;

an interlayer insulating film over at least the gate electrode; and

a source electrode and a wiring over the interlayer insulating film, wherein the source electrode is in contact with the semiconductor layer and the wiring is in contact with the gate electrode each through a contact hole opened in the interlayer insulating film,

wherein the source electrode contains a first layer and a second layer and the wiring contains a third layer and a fourth layer, [[and]]

wherein a part of the first layer, a part of the second layer, a part of the third layer and a part of the fourth layer are located over the interlayer insulating film,

wherein the first side recess is filled with the first layer,

wherein the second side recess is filled with the third layer, and

wherein the first layer is in contact with the gate insulating layer.

50. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the semiconductor layer contains crystalline silicon.

51. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the first layer contains at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony.

52. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the first layer is an alloy of aluminum and germanium.

53. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the second layer contains aluminum.

54. (Canceled)

55. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the interlayer insulating film contains at least one selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

56. (Previously Presented) The semiconductor device having a thin film transistor according to claim 49, wherein the semiconductor device is an active matrix type EL display device.